

ALLEN CHEN

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EDUCATION

Boston University, College of Engineering

Boston, MA

B.S. Electrical Engineering | GPA: 3.86 / 4.0

Expected May 2028

- Relevant Coursework: Digital VLSI Design · Microelectronics · Logic Design · Machine Learning · Signals & Systems

TECHNICAL SKILLS

EDA / PCB: Altium Designer, KiCad, Fusion 360, LTspice, PSIM

HDL & FPGA: Verilog, Vivado (synthesis, behavioral simulation, RTL verification)

Embedded & Firmware: STM32, ESP32, STM CUBE IDE, Arduino, C, C++

Simulation & Analysis: Lumerical (FDTD/MODE), MATLAB, Python, QCoDeS, Numpy, Qiskit

EXPERIENCE

Undergraduate Quantum Photonics Researcher | Lake Lab, Boston University | Boston, MA

April 2026 – Present

- Developed a HF wet-etching adiabatic taper process to narrow 8.2 μ m SMF-28e+ fibers to 2.5 μ m, achieving sub-0.1 dB coupling loss into a reverse tapered silicon waveguide inserted into erbium-doped photonic circuits.
- Engineered a room-temperature optical testing station from off-the-shelf components to characterize fiber taper profiles and measure optical coupling efficiency.
- Reduced taper geometry design iterations by ~60% employing ANSYS Lumerical FDTD/MODE simulations to pre-screen coupling efficiency across 15+ taper profiles before fabrication.

Low-Voltage Electronics Engineer | Terrier Motorsport (FSAE) | Boston, MA

Oct 2024 – Present

- Achieved first-ever electrical inspection pass by redesigning the 300 V pre-charge circuit. Replaced unreliable 555-timer topology with isolated comparator logic to improve HV inrush current control.
- Designed 4-layer STM32 CAN Watchdog PCB with impedance-controlled differential routing and hardware fault protection to monitor vehicle safety states and enforce real-time fail-safe responses.
- Validated vehicle cooling and insulation monitoring systems under live 300 V test conditions, confirming fault-detection latency under 10 ms.

Sales Engineering Intern | GW Instek | Taipei, Taiwan

Jul 2025 – Aug 2025

- Defined testing metrics for Open Compute's M-CRPS and BBU modules, using programmable AC/DC sources and loads.
- Analyzed ± 400 VDC data center power system architecture and produced a gap analysis report, mapping legacy 48V system integration points.
- Ran hands-on instrument demos for 10+ client engineering teams evaluating power and signal-integrity test setups.

R&D Intern | Semiconductor Physics Lab, National Taiwan University | Taipei, Taiwan

Jun 2024 – Aug 2024

- Fabricated MOSFET samples for Vishay e-Fuse R&D by operating electron-beam PVD and depositing Au/Ti contact layers on silicon wafers under cleanroom conditions.
- Characterized breakdown voltages and impedance profiles across sample batches; used XRD phase analysis to validate crystal structure, ensuring compound integrity before packaging.

PROJECTS

Whack-a-Mole Game | FPGA, Verilog, AMD Vivado

Apr 2026 – May 2026

- Implemented full RTL design in Verilog: LFSR-based pseudorandom mole spawn engine, time-division multiplexed 7-segment display, and a VGA state machine driving custom game graphics at 640x480.
- Synthesized and verified on Vivado with functional testbenches at each design stage.

SMT Reflow Oven for Terrier Motorsports | Control systems, Closed-loop

Nov 2025 – Dec 2025

- Converted faulty toaster oven into a production-capable SMT reflow station with a PID controlled K-type thermocouple / MAX31855 interface.
- Manually tuned PID gains based on step response observation to hold reflow profile within ± 5 °C.
- Introduced Terrier Motorsport's first in-house SMT assembly, cutting per-board hand-soldering times by up to 50%, and dramatically reducing board sizes by utilizing 0402 and 0603 package layouts.

LEADERSHIP EXPERIENCE

E-Board Secretary | BU Quantum Computing Club

July 2026 – Present

- Established official organizational status by writing a constitution and communicating with the student leadership office.
- Host weekly seminars and workshops aimed at introducing undergraduate students to quantum circuits.